

FIG. 1

FIG. 2 is a block diagram of a digital-to-analog converter (DAC) circuit. The circuit includes a digital data input (D1, D2, D3) and a latch pulse input. The digital data is processed by a series of latches (LAT1, LAT2) and switches (SW) to produce a pixel output. The circuit is controlled by a clock signal (S-CLK) and a select signal (S-SP). The output is connected to a pixel array (210) and a switch (205).

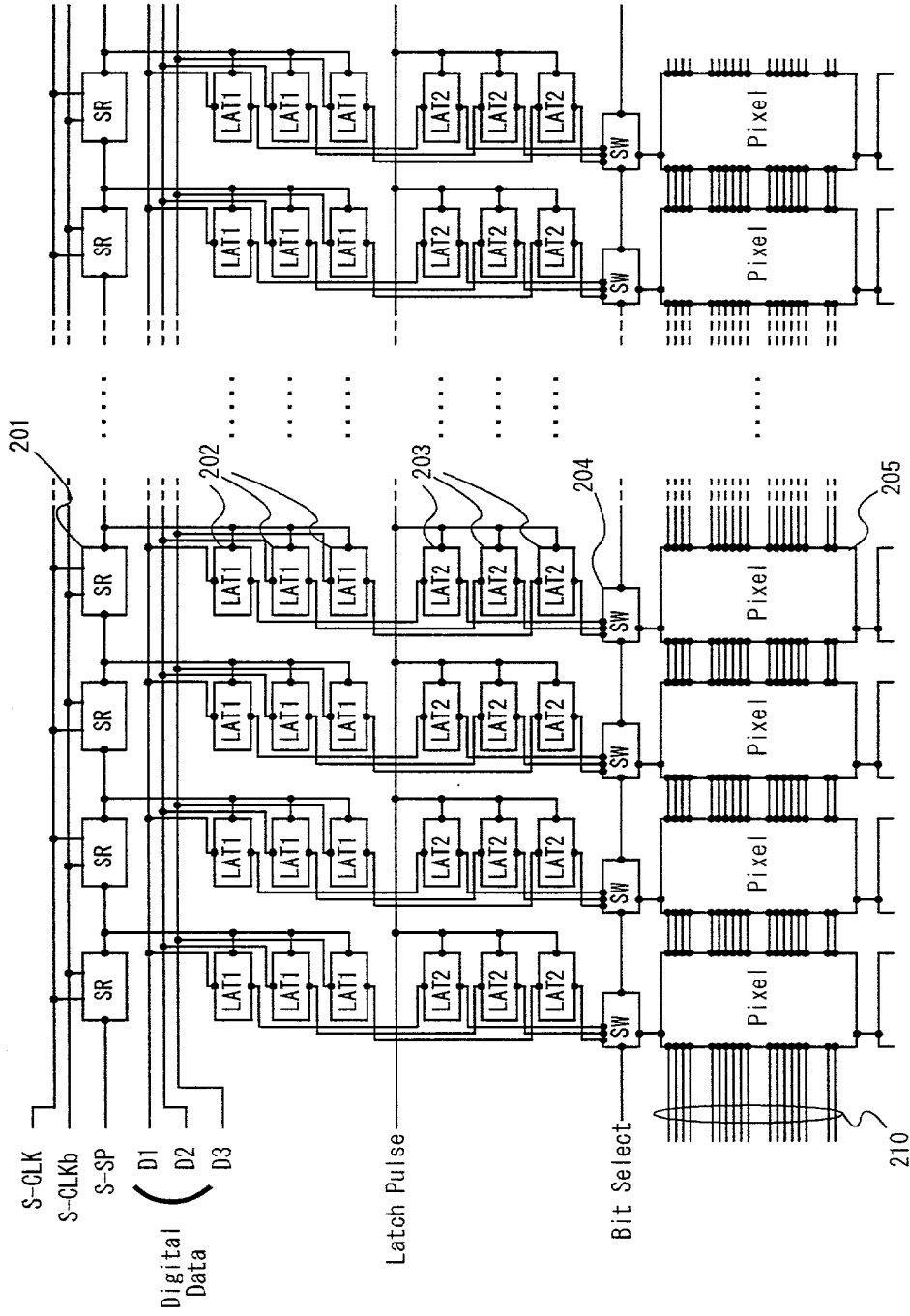


FIG. 2

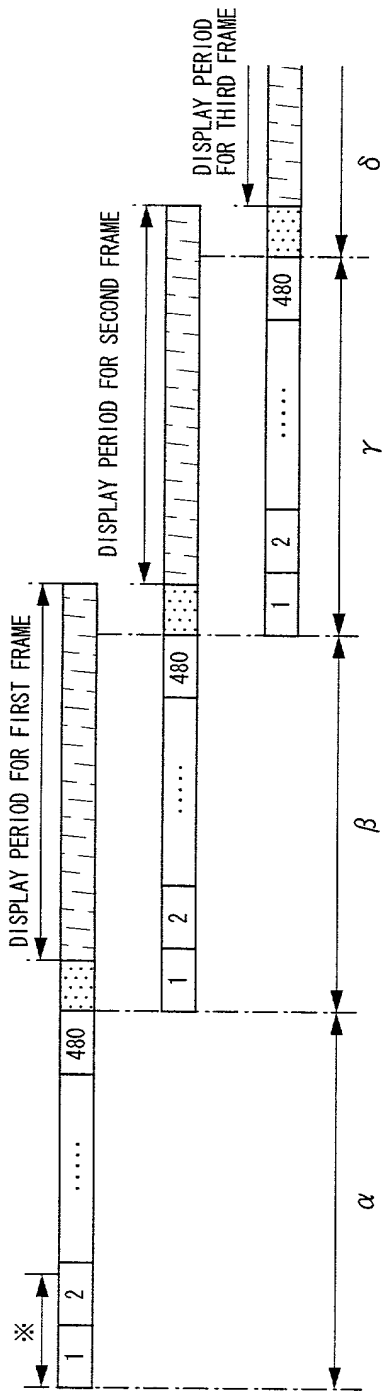


FIG. 3A

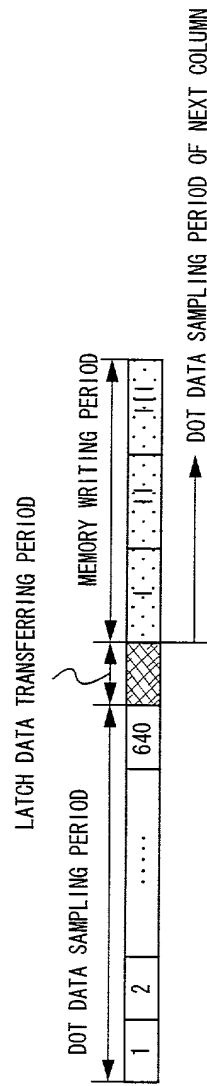


FIG. 3B

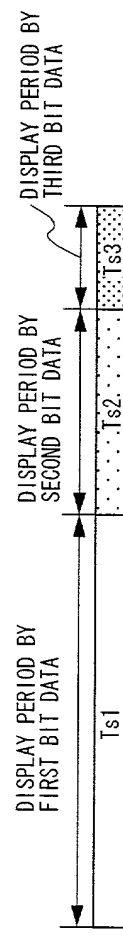


FIG. 3C

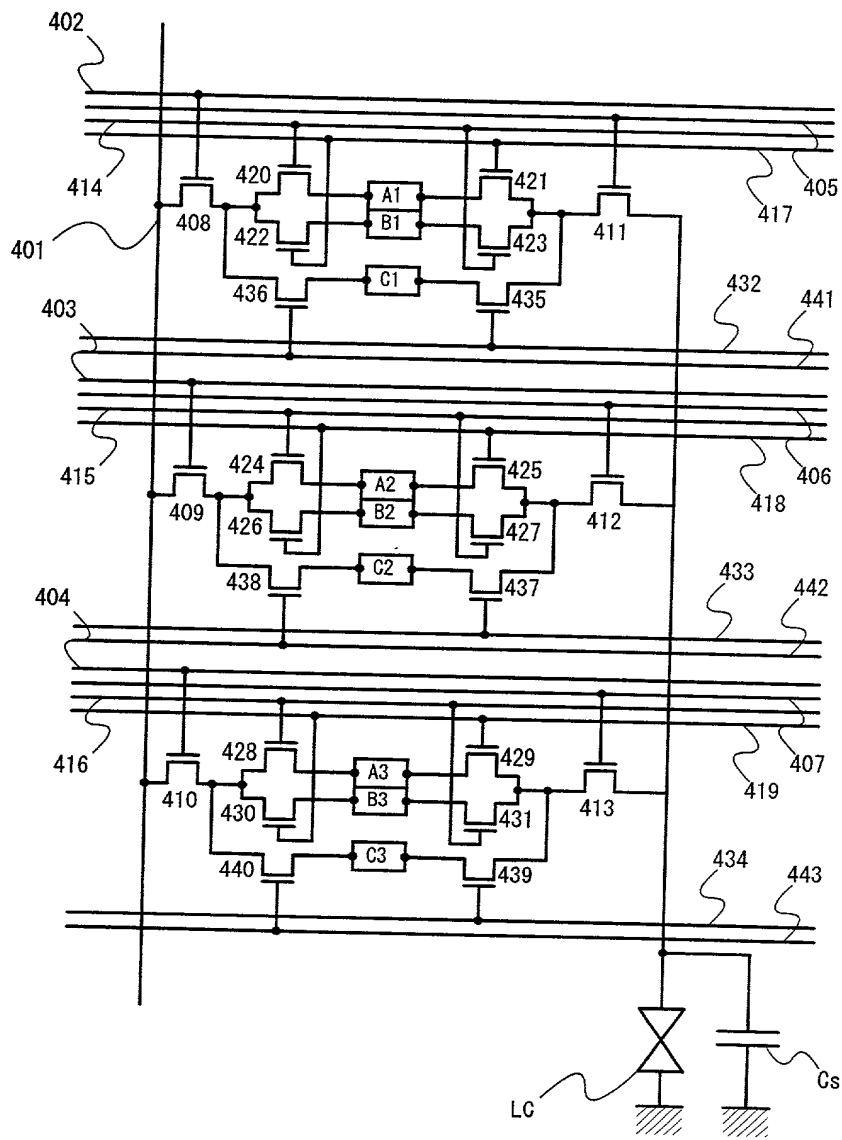


FIG. 4

FIG. 5 is a block diagram of a pixel array circuit 500. The circuit includes a plurality of pixel elements 510, each receiving a common gate voltage signal 501 and a common source voltage signal 502. The pixel elements are connected to a common drain voltage signal 503. The circuit also includes a plurality of sense amplifiers 520, each receiving a common sense voltage signal 521 and a common sense current signal 522. The sense amplifiers are connected to a common sense output signal 523. The circuit is controlled by a plurality of control signals 530, including a clock signal 531, a data signal 532, and a reset signal 533.

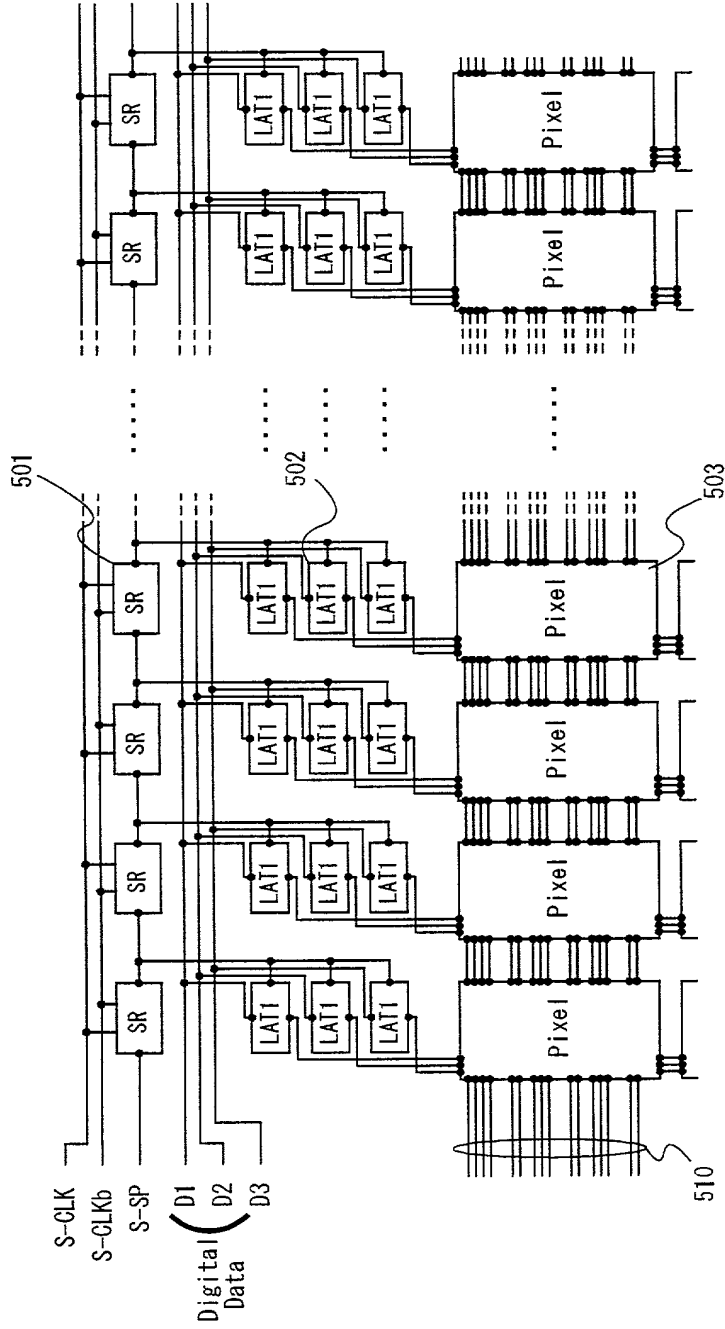


FIG. 5

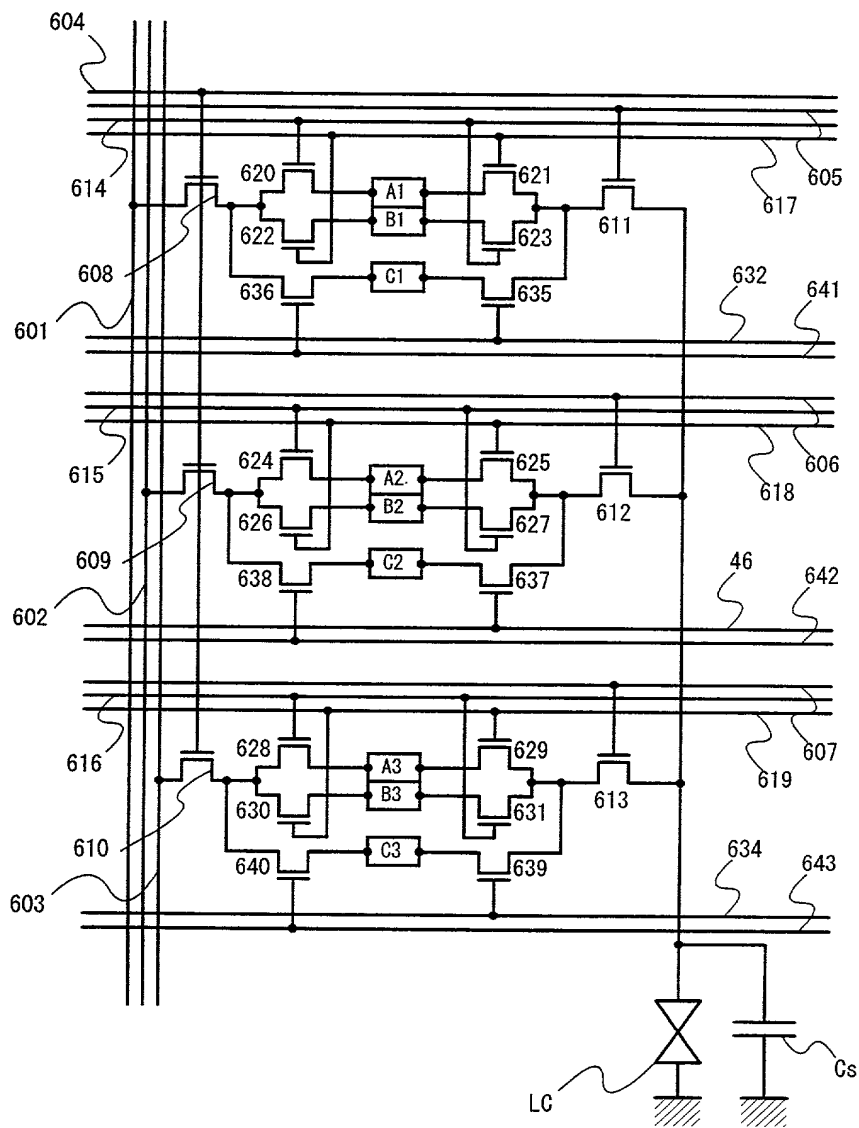


FIG. 6



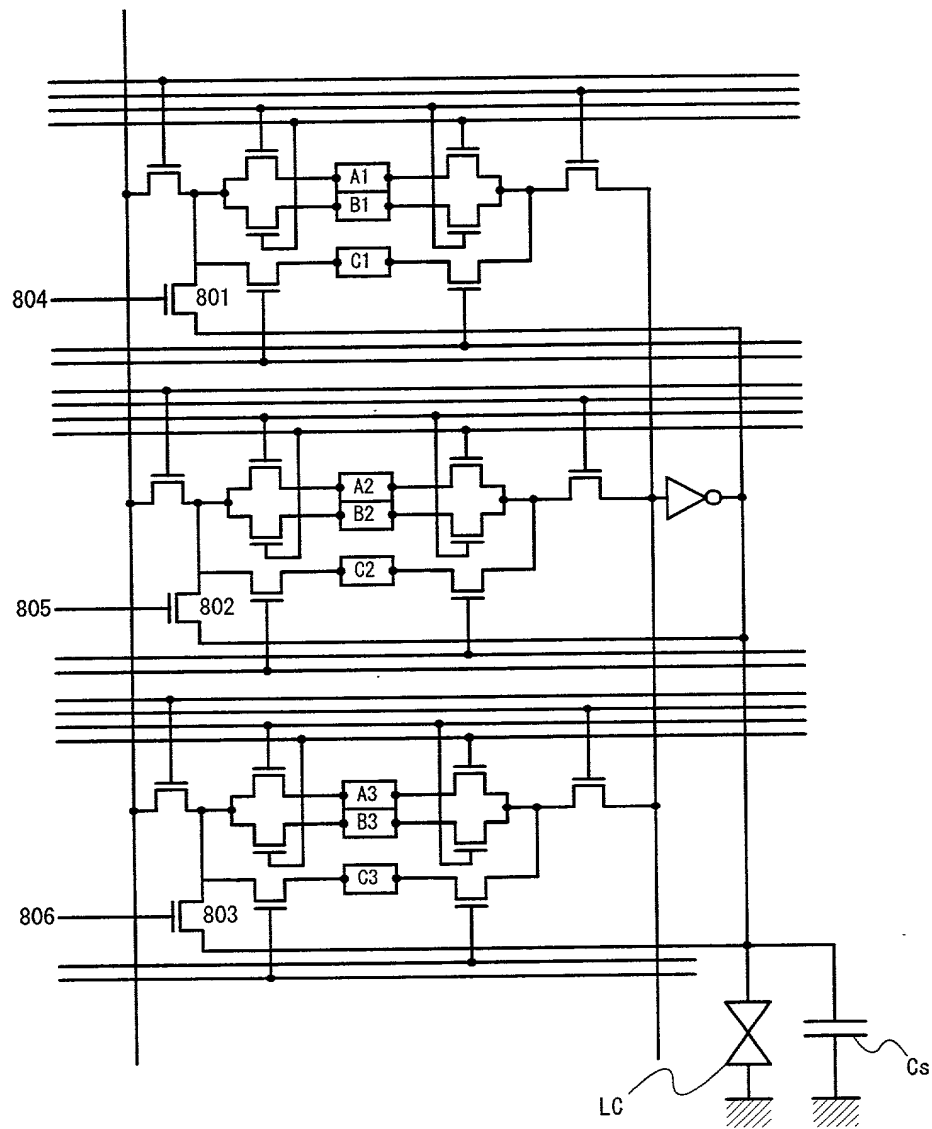


FIG. 8



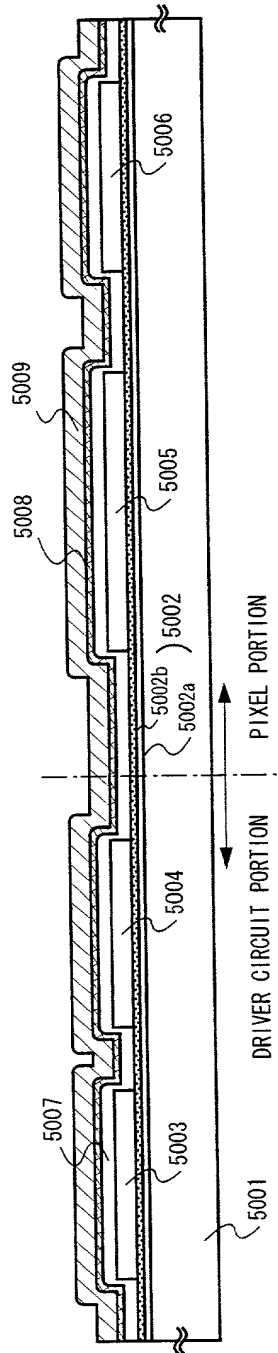


FIG. 9A

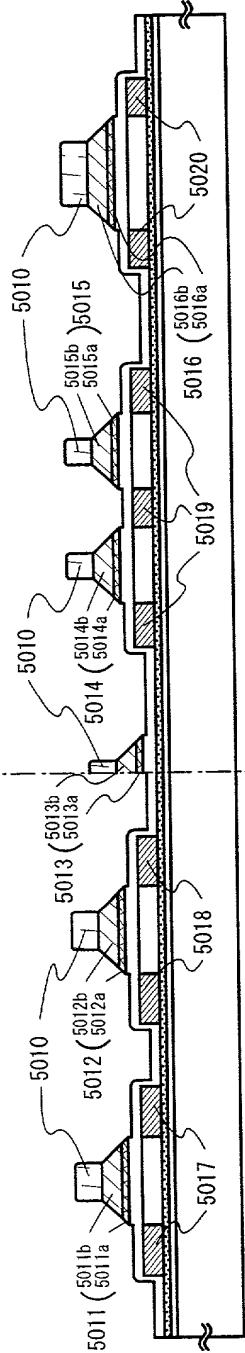


FIG. 9B

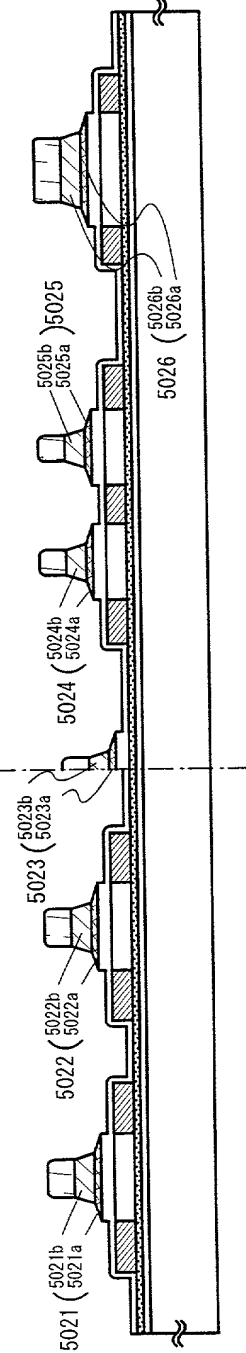


FIG. 9C

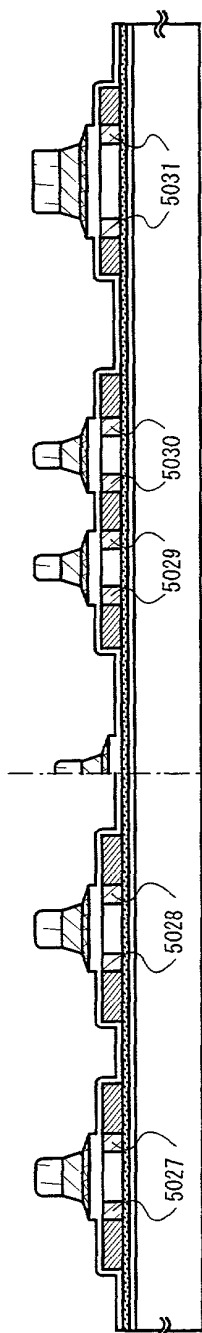


FIG. 10A

DRIVER CIRCUIT PORTION

PIXEL PORTION

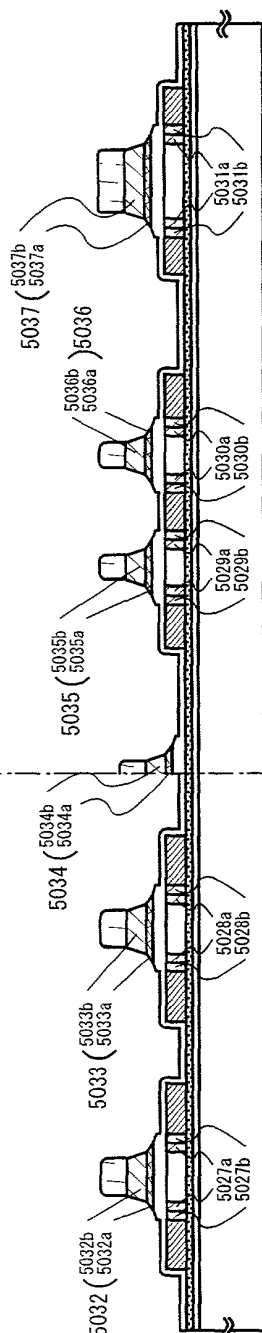


FIG. 10B

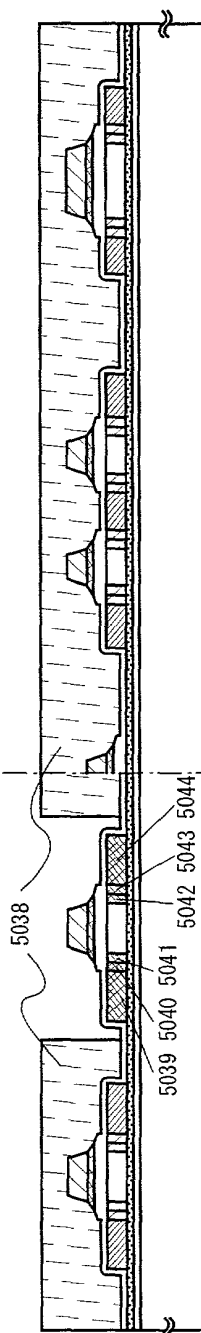


FIG. 10C

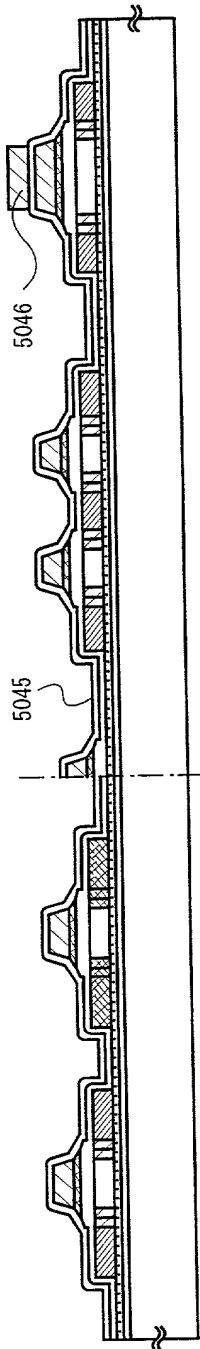


FIG. 11A

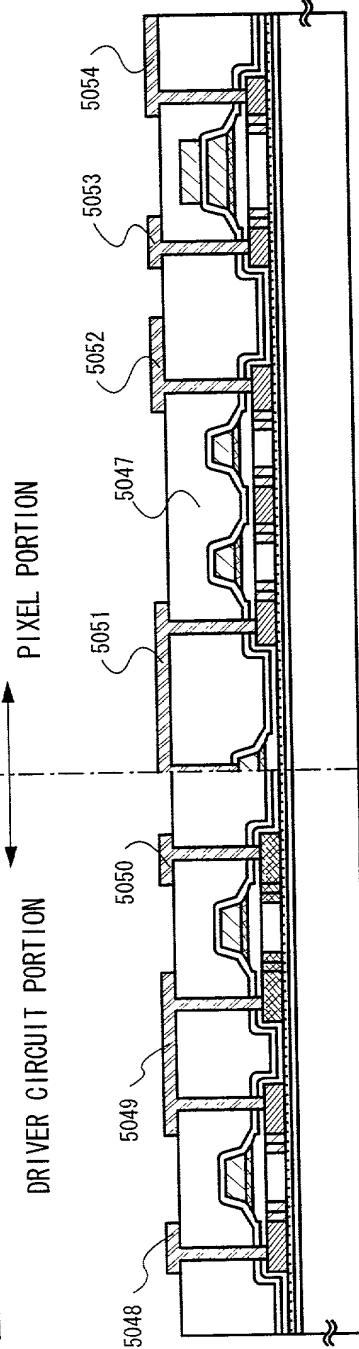


FIG. 11B

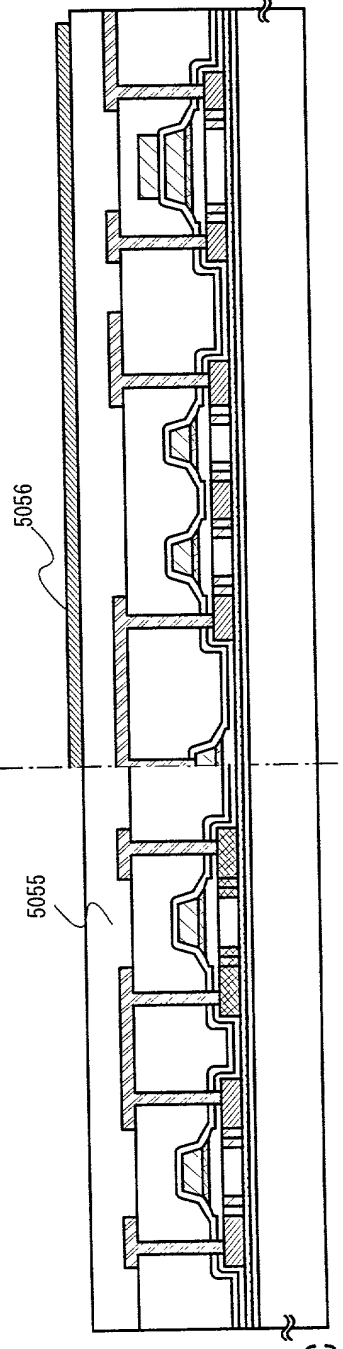


FIG. 11C

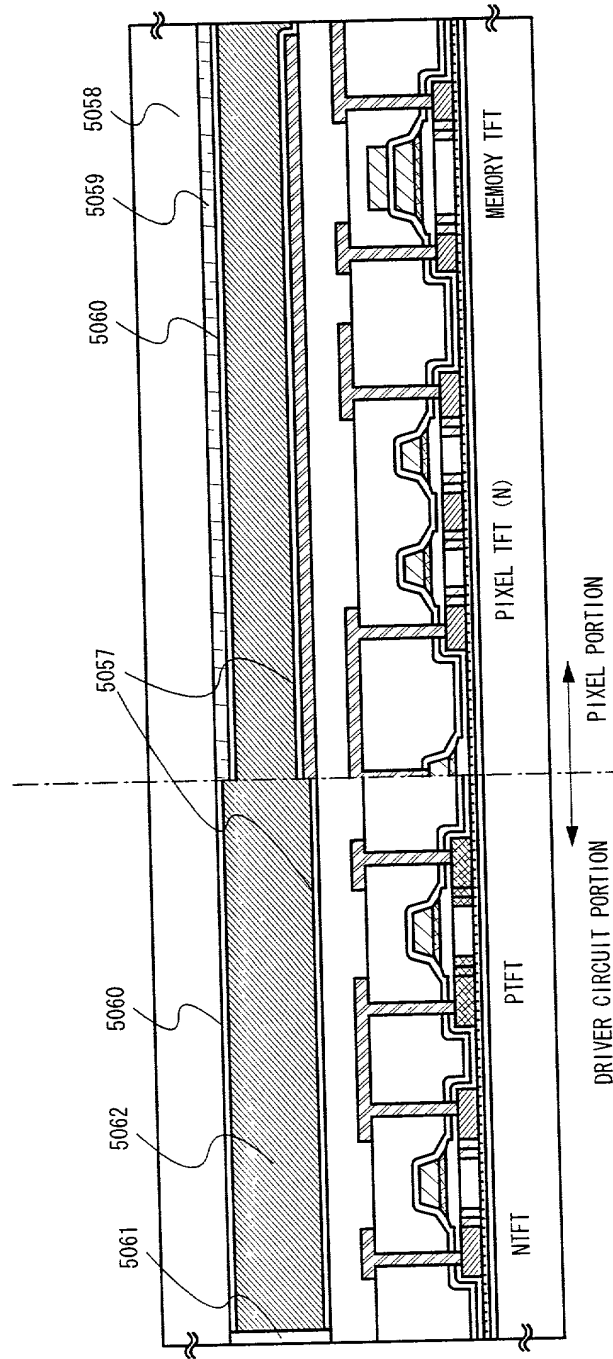


FIG. 12

FIG. 13 is a block diagram of a source signal line driver circuit 1301. The circuit includes a shift register circuit 1303, a first latch circuit 1304, a second latch circuit 1305, a D/A converter circuit 1306, and an analog switch 1307. The shift register circuit 1303 receives S-CLK and S-SP signals. The first latch circuit 1304 receives Digital Data. The second latch circuit 1305 receives Latch Pulse. The D/A converter circuit 1306 receives Vref. The analog switch 1307 is controlled by G-CLK and G-SP signals. The output of the analog switch 1307 is connected to the gate signal line driver circuit 1302. The gate signal line driver circuit 1302 is connected to the gate signal line 1308. The pixel portion 1308 is connected to the gate signal line 1308.

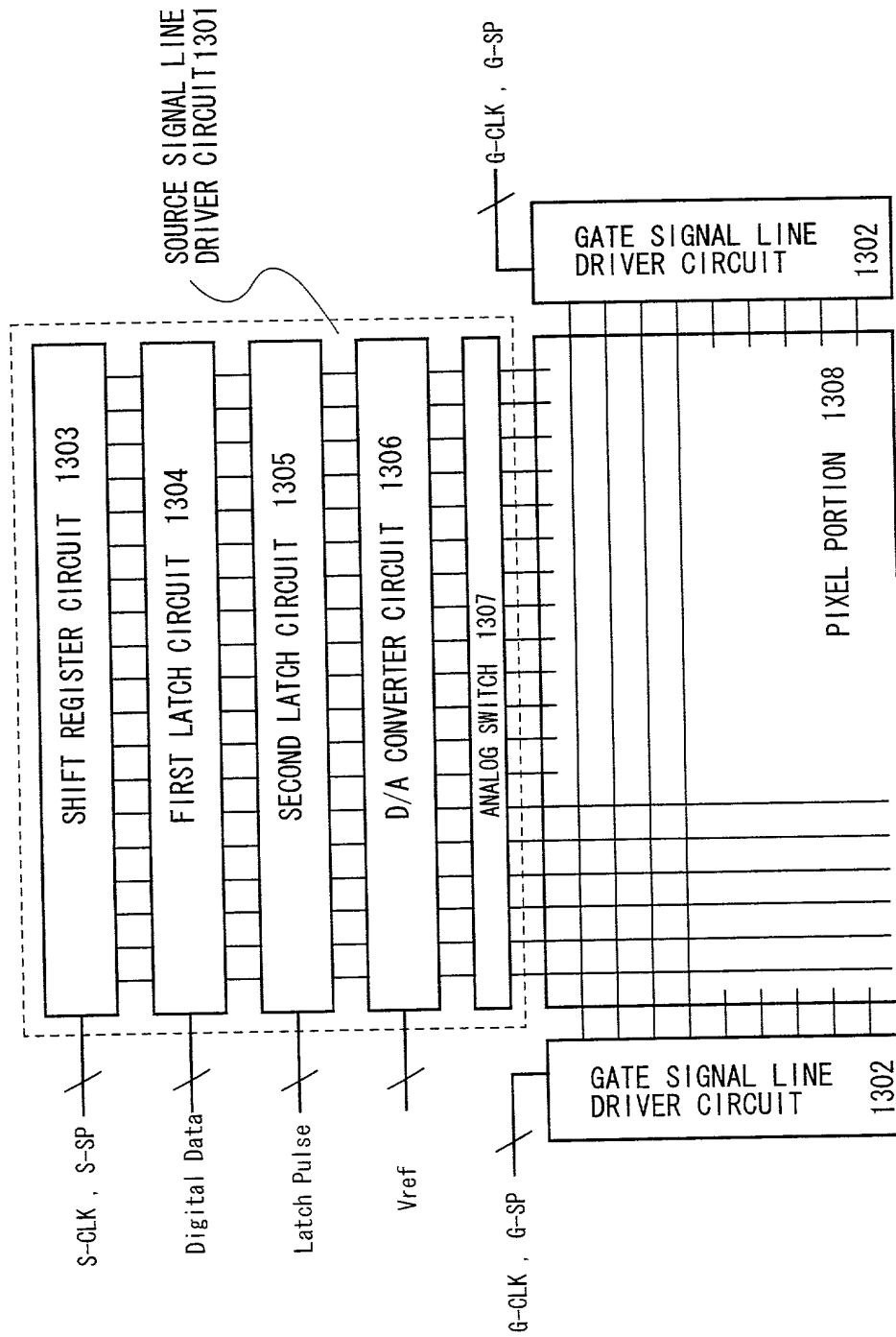


FIG. 13

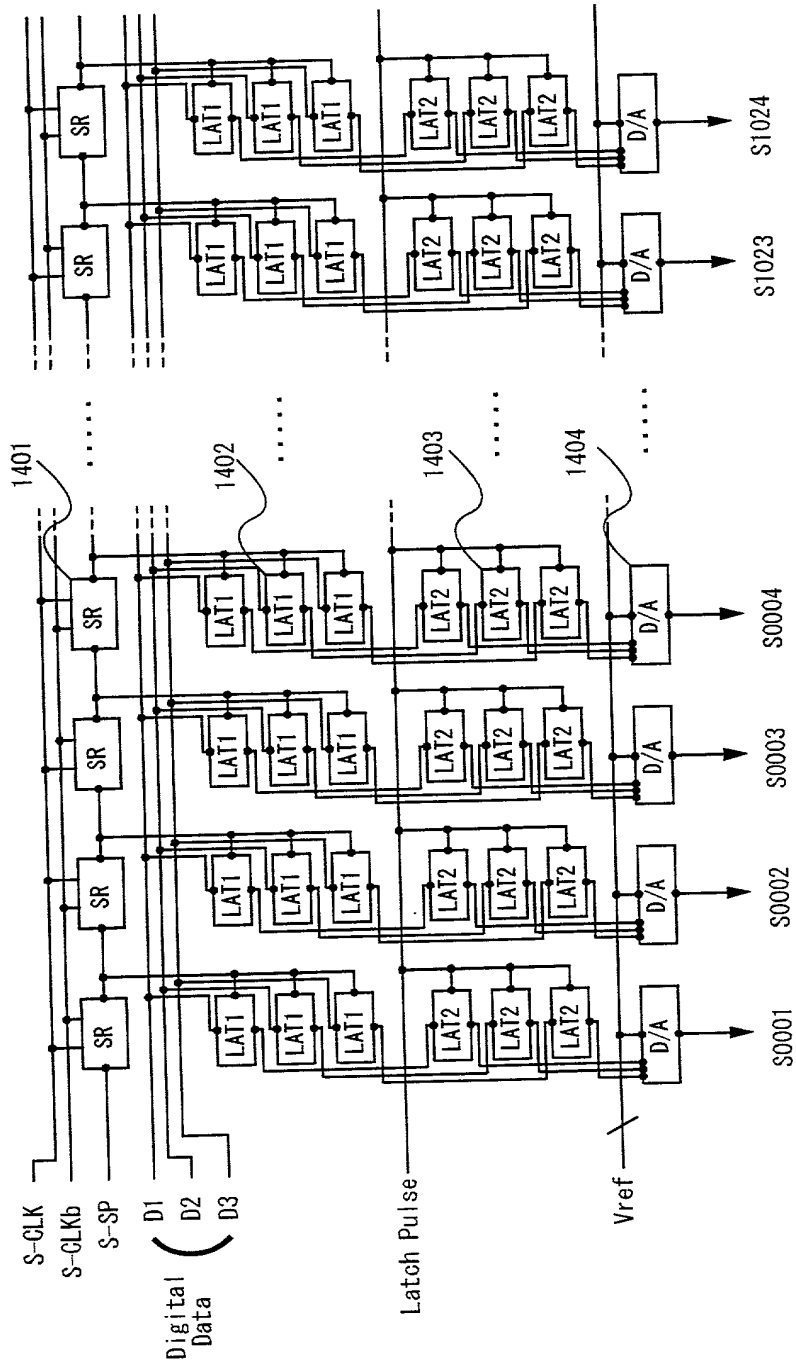


FIG. 14

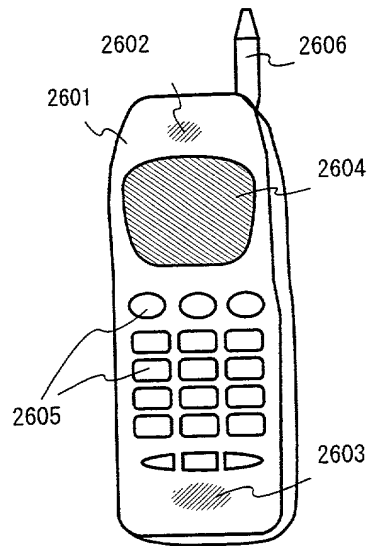


FIG. 15A

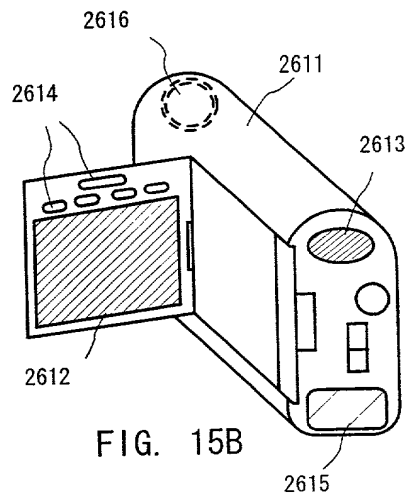


FIG. 15B

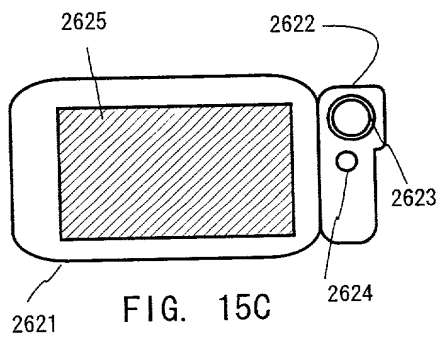


FIG. 15C

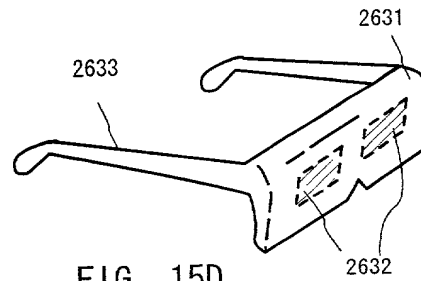


FIG. 15D

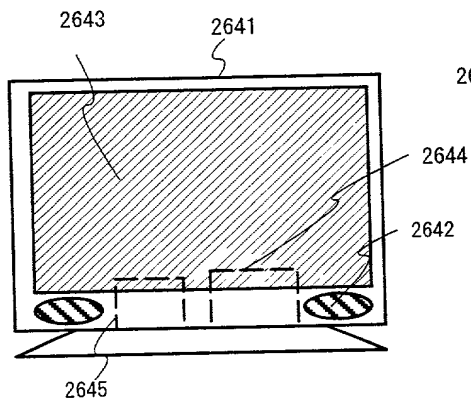


FIG. 15E

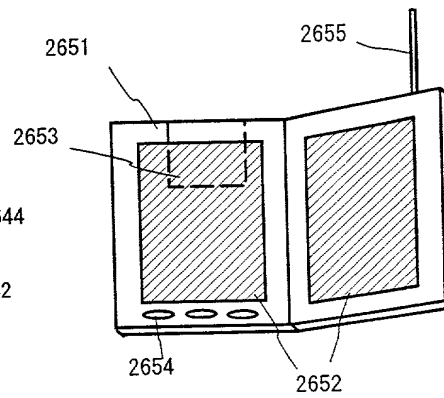


FIG. 15F

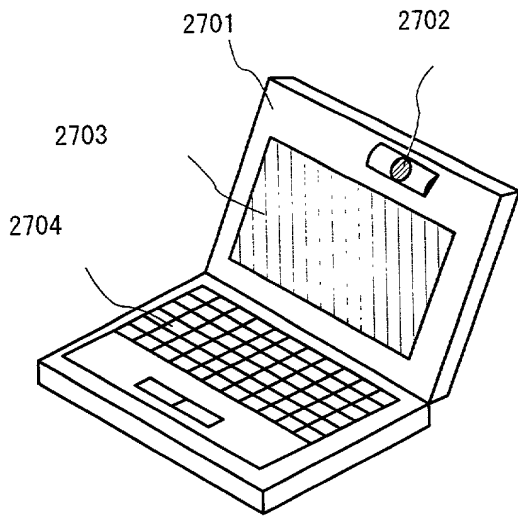


FIG. 16A

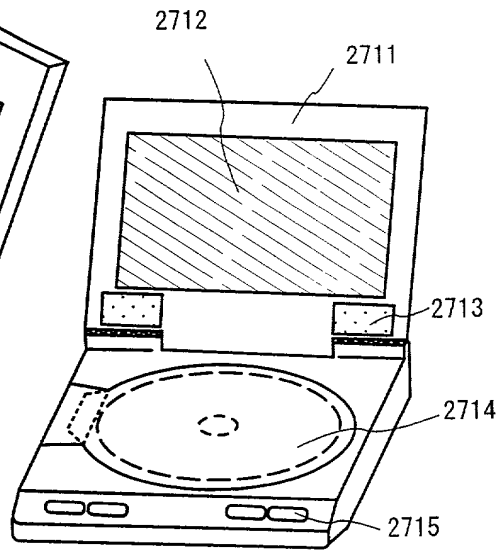


FIG. 16B

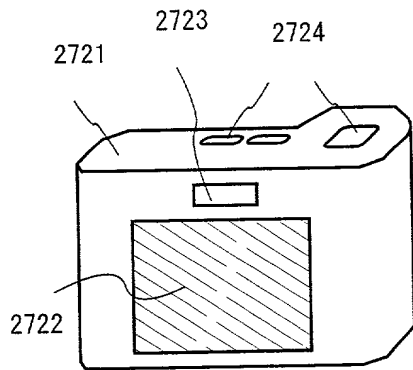


FIG. 16C

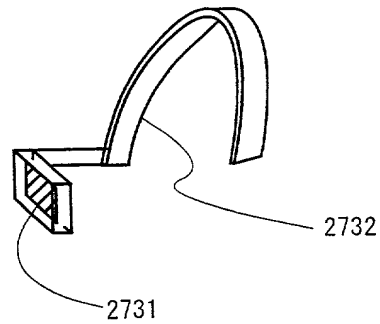


FIG. 16D



FIG. 17 is a schematic diagram of a pixel array circuit. The circuit includes a series of SR latches (1701) connected to a common S-CLK line. Each SR latch is also connected to a common S-CLKb line and a common S-SP line. The output of each SR latch is connected to a LAT1 line. The LAT1 lines are connected to a series of LAT1 latches (1702). The output of each LAT1 latch is connected to a SW line. The SW lines are connected to a series of SW latches (1703). The output of each SW latch is connected to a Pixel line. The Pixel lines are connected to a series of Pixel blocks (1704). The Pixel blocks are connected to a common 1710 line. The circuit is controlled by a Latch Pulse signal.

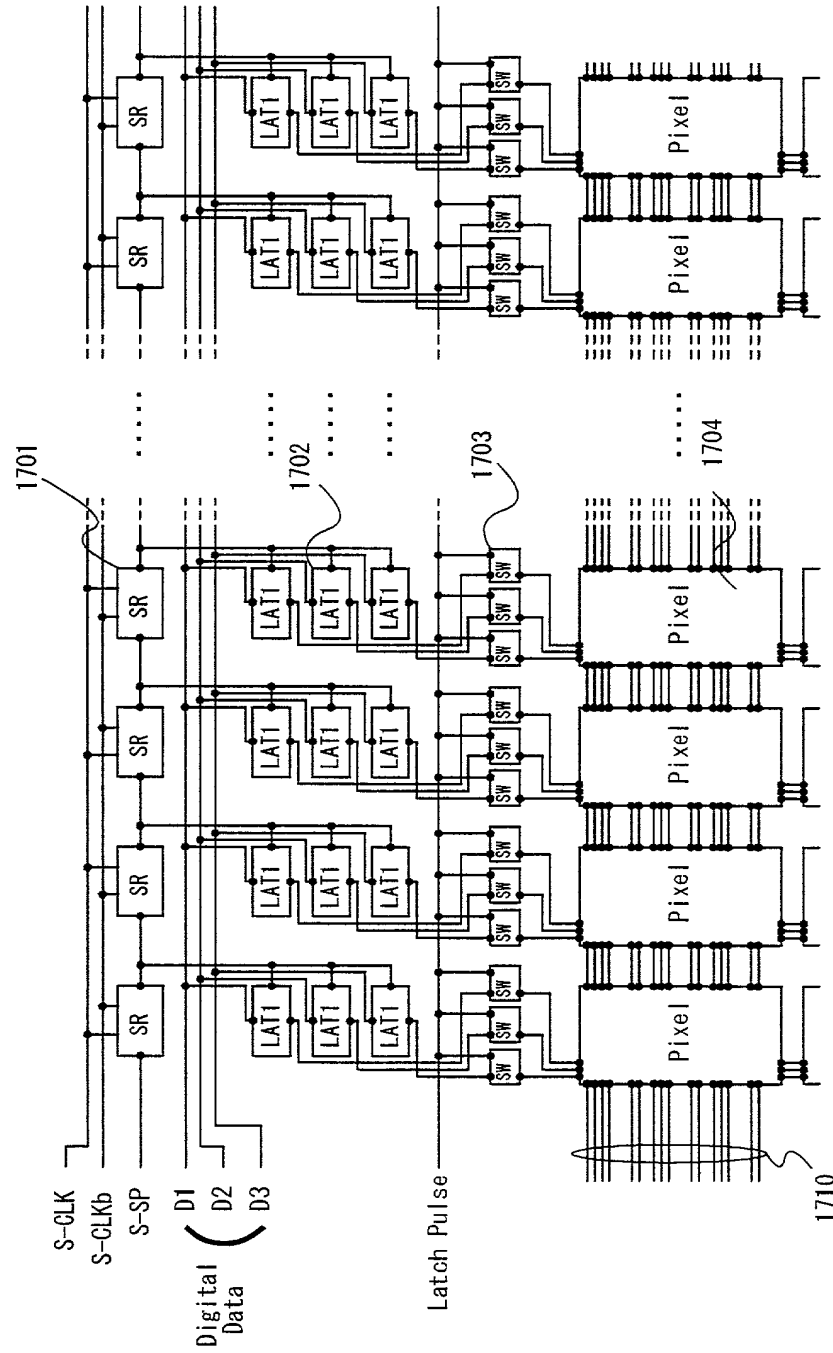


FIG. 17

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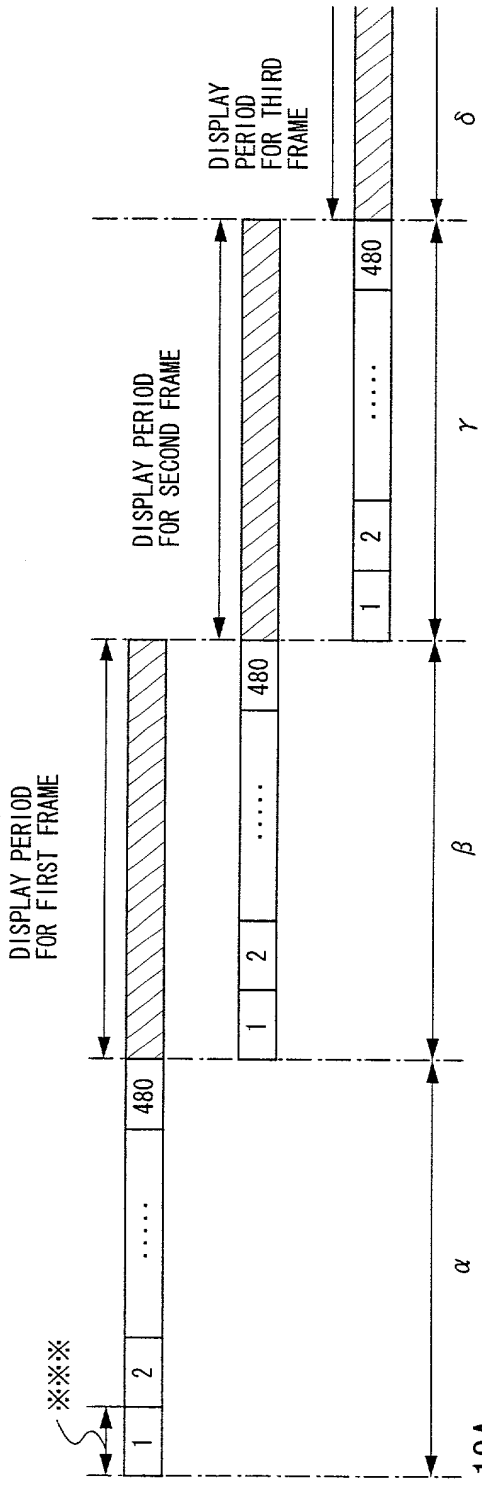


FIG. 18A

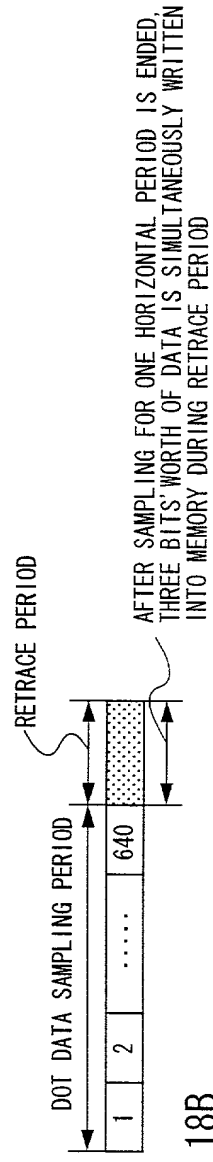


FIG. 18B

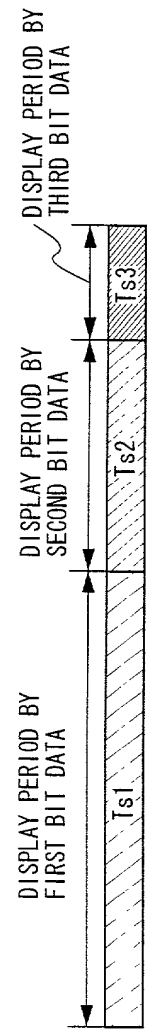
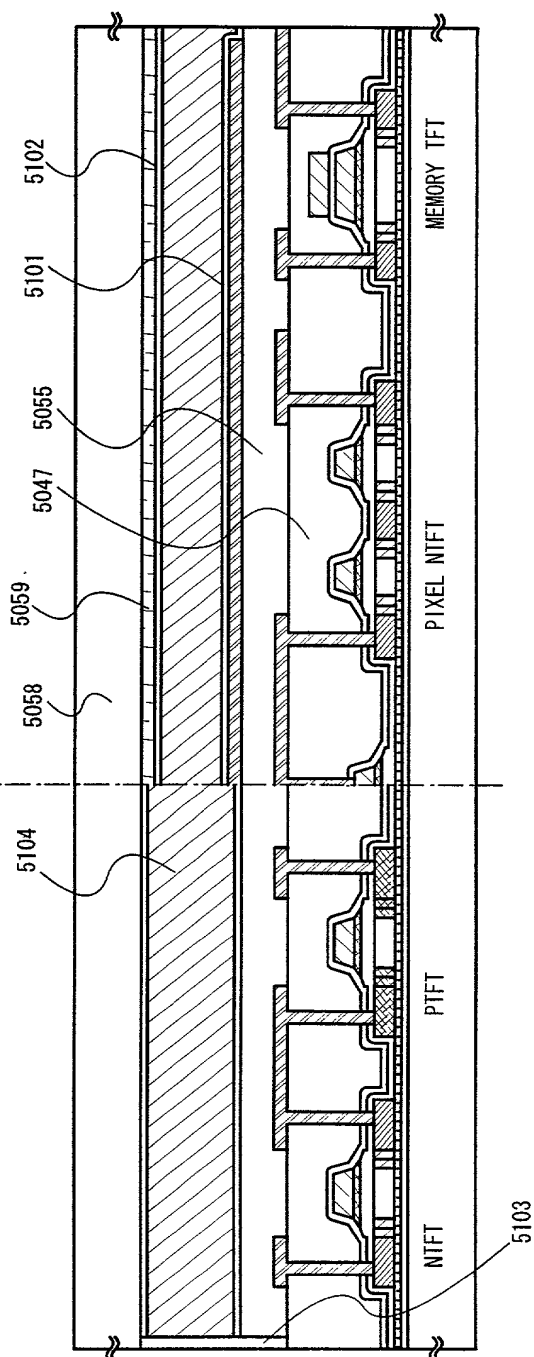
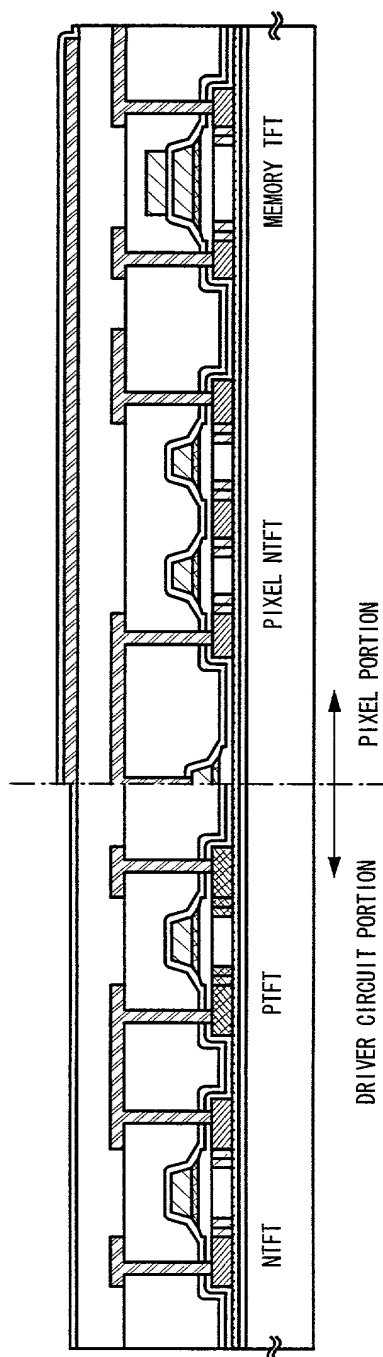


FIG. 18C



ADDRESS LINE

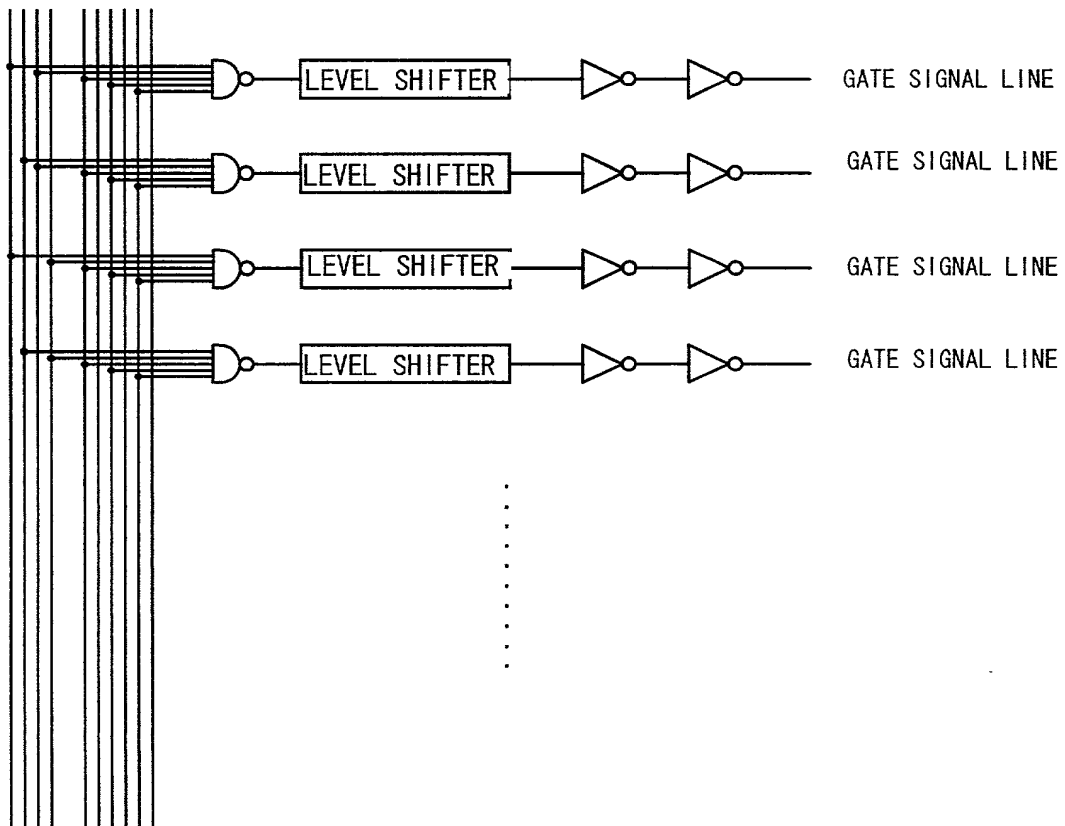


FIG. 20



FIG. 22 is a block diagram of a system 2200. The system 2200 includes a power source 2204, a microphone 2208, a speaker 2214, a speech processing circuit 2202, an external interface port 2205, a transmit-receive circuit 2215, a CPU 2206, a memory card 2203, a keyboard 2201, a video signal processing circuit 2207, a tablet interface 2218, a VRAM 2211, a DRAM 2209, a flash memory 2210, an LCD controller 2212, a gate driver circuit 2213, a source driver circuit 2213, and a pixel 2213.

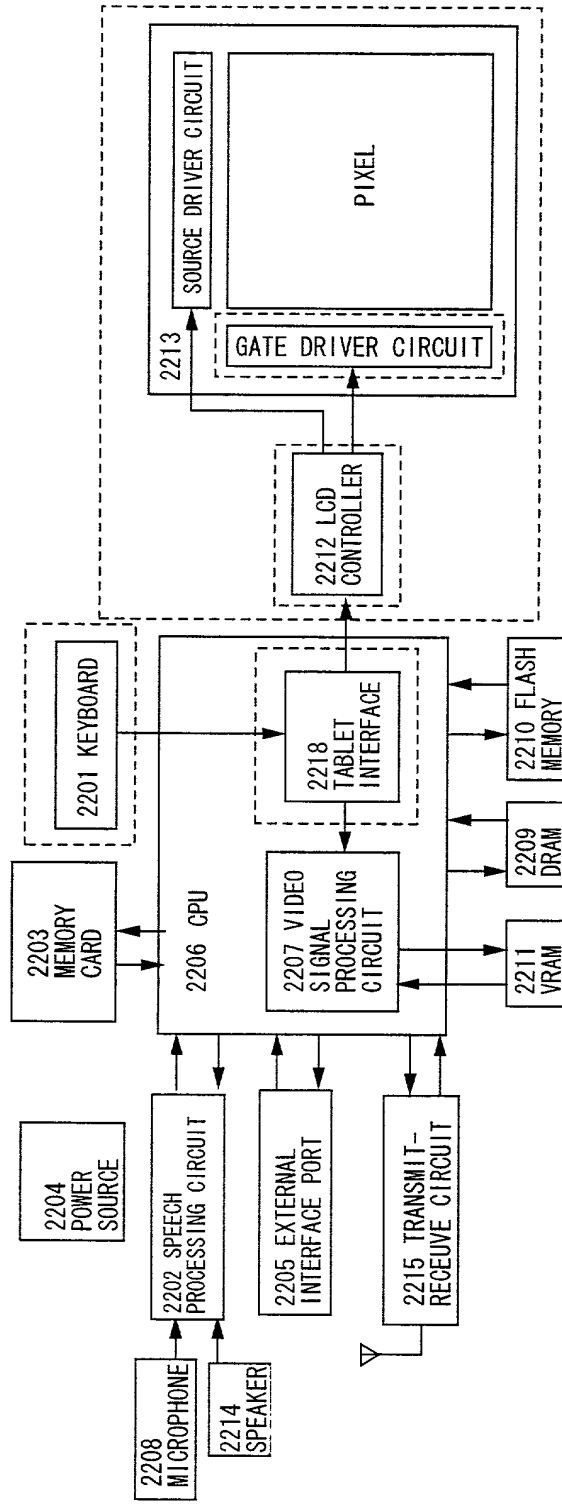


FIG. 22

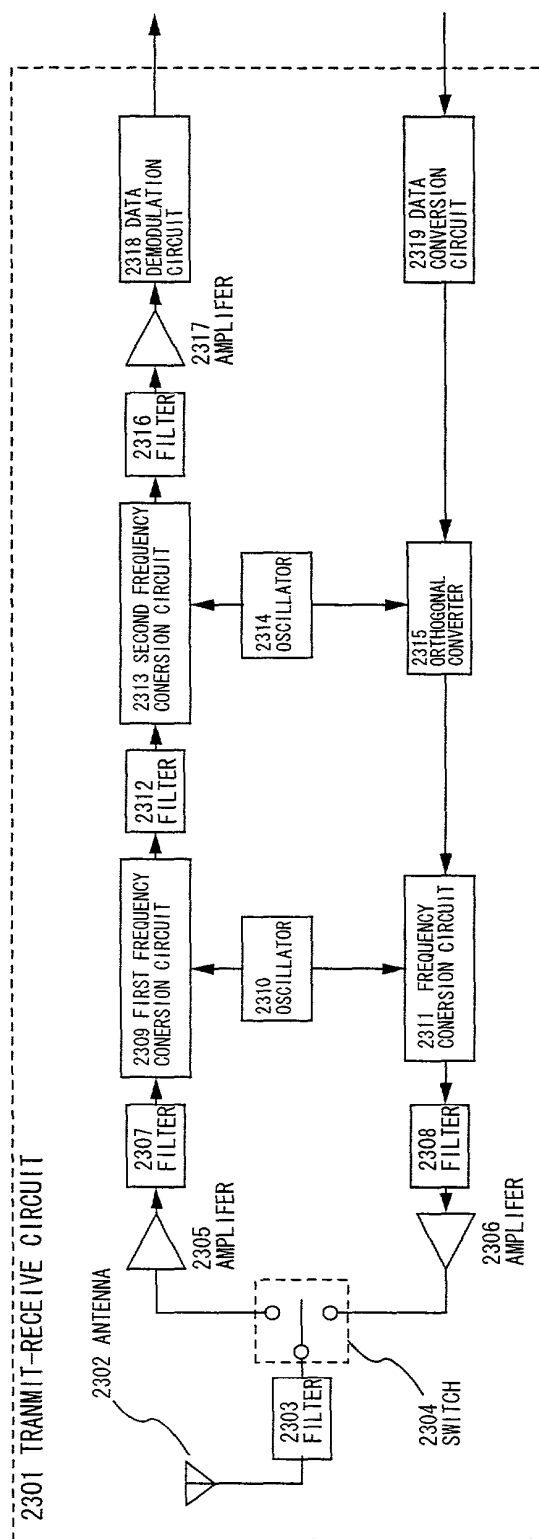


FIG. 23